



Small Satellites Systems and Services – The 4S Symposium Abstract Submission (Deadline 8.1.2008)

Title of the paper

The Core Avionics System for the DLR Compact-Satellite Series

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Summary of the paper

The SSB (Standard Satellite Bus) core avionics is a further step in the development line of the software and hardware architecture which was first used in BIRD (Bispectral InfraRed Detector). The next step improves dependability, flexibility and simplicity of the whole core avionics system. Important aspects of this concept were already implemented, simulated and tested in other ESA and industrial projects. Therefore we can say the basic concept is proven.

The main risk factors in a typical core avionics development are the complexity, software-hardware interfaces and the difficulties to handle many different interfaces in a single system. The new core avionics concept targets these problems and aims to provide a very simple integrated solution of software and hardware. The border between both shall vanish. This concept can handle both; bus control and payload control in one system.

The emerging and fast growing FPGA technology allows us to implement the biggest part of the core avionics in software, including classical CPU software and FPGA software. The use of fixed hardware is kept to a minimal limit.

In this concept the core avionic functionality is provided by a network of services. Some of them are implemented in classical CPU-software, some in FPGA-software and some in hardware devices, for example sensors and actuators. To access any service there shall be no difference in how it was implemented (CPU, FPGA, hardware) and where it runs. The core avionics system is a distributed computer system. No single node is required to be dependable. The computers are connected by a dependable hardware network which is the heart of the system. Software services can be distributed on all computers and may migrate from one to another for example in case of failures, overloading or for power management.